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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,006	03/02/2004	John T. Moore	4305.2US (99-1251.02/US)	1271

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,006	MOORE ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on March 17, 2005. Claims 1-40 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al (6,033,998) taken with Mukhopadhyay (6,399,448) and Barsan (5,942,780).

Aronowitz teaches a method for hardening at least a portion of a gate oxide layer on a silicon substrate comprising at least the steps of: forming an oxide layer 206a/206b over the substrate 202; forming a resist layer (Fig 2D) over at least a portion of the oxide layer; patterning the resist layer to create at least at least one exposed area of the oxide layer 206b (Fig 2D; col 5, line 45 through col 7); hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening (RPN) treatment to create at least one hardened area within the oxide layer and at least one non-hardened area within the oxide layer (col 5, line 67 through col 6; Fig 2D), at a temperature of about 60°C (col 6, lines 40-52); and thermally growing at least a portion of the at least non-harden area with the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer (col 6, lines 61-67; Fig 2F), wherein a CMOS device of an integrated circuit including N-channel and P-channel devices (col 2, lines 60-63; lines 8-10). Re further claims 24,4,10,17,30,37,1 wherein, hardening the at least one exposed area of the oxide layer uses a remote plasma nitrogen hardening (RPN) treatment to create at least one hardened area within the oxide layer and at least one non-hardened area (col 6, lines 1-50). Re further claims 26,6,12,19,26,32,39, wherein the oxide layer 206 has a thickness of 25 angstroms (col 5, lines 58-65).

Aronowitz lacks patterning a second resist pattern and hardening the second exposed area of the oxide layer, as recited in claim 21 and other independent claims.

However, Mukhopadhyay teaches forming resist layers and patterning to form a first resist pattern 24 (Fig 1) and a second resist pattern 34 (Fig 2) over a portion of the oxide layer to exposed a first area of the oxide layer 12 (Fig 1) and a second area of the oxide layer 12 (Fig 2),

and hardening the first exposed area of the oxide layer 12 (Fig 1), and hardening the second exposed area of the oxide layer 12 (Fig 2; col 4, line 8-67), wherein a plurality of areas are exposed and a plurality of thick oxide and thinner oxides 32,42,22 are formed on the substrate (Fig 4; col 5). Additionally, Barsan teaches forming resist layers and patterning to form a first resist pattern 75 (Fig 4a) and a second resist pattern 4b (Fig 4b; col 8, line 64 through col 9) over a portion of the oxide layer 71 to exposed a first area of the oxide layer (Fig 4a) and a second area of the oxide layer (Fig 4b), and hardening the first exposed area of the oxide layer and hardening the second exposed area of the oxide layer by nitrogen implantation, wherein a plurality of areas are exposed and a plurality of thick oxide and thinner oxides 27,47,55 are formed on the substrate (Fig 4d).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thick and thin oxide layer of Aronowitz by forming a second resist pattern and hardening the second exposed area of the oxide layer, as taught by Mukhopadhyay and Barsan. This is because of the desirability to form an oxide layer having a plurality of first thick oxide, a second thinner oxide layer 42, and a third thinner oxide layer 22 on the semiconductor substrate (Fig 4) so that a plurality of transistors having high voltage and low voltages can be formed of the same substrate at the same time.

Re further claims 5,11,18,25,31,38, Aronowitz teaches (at col 6, lines 5-60) the plasma nitrogen hardening is performed at a temperature of about 60°C (col 6, lines 40-52; and col 7, lines 35-50), a power of 200 W, for a period of time of 120 seconds so as a desired thickness of the oxide layer can be formed. Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of parameters, as taught by Aronowitz, and in the semiconductor art, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934). Re further claim 35, wherein

using these high speed and low power consumption transistors to form a dynamic random access memory device would have been obvious to one of ordinary skill in the art.

Response to Amendment

** Applicants' remarks filed March 17, 2006 with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Aronowitz et al, as a primary reference, already teach hardening treatment by using a plasma nitrogen, wherein a temperature is about 60°C for nitrogen plasma treatment, which temperature is approximately less than 90°C as claimed.

Under 35 USC 103 rejection, in combination of the references, the secondary references including Mukhopadhyay and Barsan prima facie teach the use of a second resist layer in addition to the use of the first resist layer because of the desirability to form the oxide layer having a plurality of oxide regions having different thicknesses on the same semiconductor substrate, namely, a first thick oxide, a second thinner oxide layer, and a third thinner oxide layer. By doing that, a plurality of transistors having high voltage and low voltages can be formed on the same semiconductor substrate at the same time.

The rejection is outstanding and maintained.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-1,5,6,102

Michael Tibbits
Primary Examiner